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EXAMINER	
LEE, CHEUNG	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 08/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/765,393	CAMPBELL, KRISTY A.	
	Examiner	Art Unit	
	Cheung Lee	2812	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *61-119* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *61-119* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/21/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on June 21, 2004 was filed before the first action on the merits. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 61, 73, 89, 93, 99, and 107 are rejected under 35 U.S.C. 102(b) as being anticipated by Kozicki et al. (U.S. Patent 6,084,796; hereinafter "Kozicki").

3. With respect to claim 61, Kozicki discloses a method of forming a memory element (col. 5, lines 3-17), said method comprising: forming at least one resistance variable material layer (col. 5, lines 18-36); forming at least one metal-containing layer adjacent said resistance variable material (col. 6, lines 11-25); and forming at least one conducting channel within said resistance variable material layer by applying a conditioning voltage to the memory element (col. 5, lines 51-67).

4. With respect to claim 89, Kozicki discloses a method of forming a memory element (col. 5, lines 3-17), said method comprising forming at least one doped chalcogenide glass layer (col. 5, lines 18-36) with polarizable metal-chalcogen regions within a glass backbone (col. 5, lines 18-50); electrically coupling first and second electrodes (col. 5, lines 51-67; col. 8, lines 1-15) to said doped chalcogenide glass layer (fig. 1B, item 12); and polarizing said metal-chalcogen regions with a conditioning voltage applied to said electrodes to form at least one conducting channel comprising said polarized metal-chalcogen regions (col. 5, line 51-col. 6, line 42), said conducting channel configured to receive and expel metal ions in response to write, erase and read voltages applied to said memory element (col. 12, lines 20-49). Kozicki discloses usage of a chalcogenide-metal ion composing a chalcogenide material and a metal (col. 5, lines 18-36), and formation of a conductive dendrite within chalcogenide glass with an applied voltage, and also the transportation of metal ions (col. 5, lines 51-67), so the examiner takes the position that the steps of receiving and expelling metal ions are inherently performed when write, erase and read voltages are applied.

5. With respect to claim 99, Kozicki discloses a method of forming a memory element (col. 5, lines 3-17), said method comprising forming at least one chalcogenide glass layer (col. 5, lines 18-36); forming at least one metal-containing layer (col. 6, lines 11-25) over said chalcogenide glass layer (fig. 4A, item 22); electrically coupling first and second electrodes (col. 5, lines 51-67; col. 8, lines 1-15) to said chalcogenide glass layer (fig. 4A, item 22); and applying a conditioning pulse (col. 3, lines 48-55) to the memory element to bond regions of metal and glass within said chalcogenide glass layer (col. 5, lines 37-67), said bonded regions forming at least one conducting channel within said chalcogenide glass layer (col. 5, lines 51-col. 6, line 42).

6. With respect to claims 73, 93, and 107, Kozicki discloses a method of forming a memory element as set forth in claims 61, 89, and 99, wherein prior to applying said conditioning voltage, said memory element has a first resistance state and after applying said conditioning voltage to said memory element, said memory element has a second resistance state lower than said first resistance state (fig. 2; col. 6, lines 55-67).

7. Claims 61-63, 89, 96-99, and 113-115 are rejected under 35 U.S.C. 102(e) as being anticipated by Campbell et al. (U.S. Publication 2004/0042259; hereinafter "Campbell")

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

8. With respect to claim 61, Campbell discloses a method of forming a memory element (page 2, paragraph 22; fig. 1; hereinafter refer to fig. 1 for figure's item numbers), said method comprising: forming at least one resistance variable material layer (17; page 2, paragraph 25); forming at least one metal-containing layer adjacent said resistance variable material (18; page 2, paragraph 29); and forming at least one conducting channel within said resistance variable material layer by applying a conditioning voltage to the memory element (page 1, paragraphs 3-5). Since like in the conventional practice, Campbell uses germanium-selenide glass doped with silver for resistance variable material, the examiner takes the position that the step of forming a

conducting channel or a dendrite within the resistance variable material under the influence of the applied voltage is inherently performed (page 1, paragraphs 3-5).

9. With respect to claim 89, Campbell discloses a method of forming a memory element (page 2, paragraph 22; fig. 1), said method comprising forming at least one doped chalcogenide glass layer (page 2, paragraphs 26-27) with polarizable metal-chalcogen regions within a glass backbone (page 2, paragraph 27); electrically coupling (24) first and second electrodes (14 and 22) to said doped chalcogenide glass layer (17); and polarizing said metal-chalcogen regions with a conditioning voltage applied to said electrodes to form at least one conducting channel comprising said polarized metal-chalcogen regions (page 1, paragraphs 3-5), said conducting channel configured to receive and expel metal ions in response to write, erase and read voltages applied to said memory element (page 3, paragraphs 36 and 37). Campbell discloses usage of germanium selenide glass layer and silver selenide layer and formation of a conductive dendrite within chalcogenide glass receiving silver ions; the change in resistance is the result of the movement of conductive silver dopant due to the applied voltage (page 1, paragraphs 3-6), so the examiner takes the position that the steps of receiving and expelling metal ions are inherently performed when write, erase and read voltages are applied.

10. With respect to claim 99, Campbell discloses a method of forming a memory element (page 2, paragraph 22; fig. 1), said method comprising forming at least one chalcogenide glass layer (page 2, paragraph 26); forming at least one metal-containing layer (18) over said chalcogenide glass layer (17); electrically coupling (24) first and second electrodes (14 and 22) to said chalcogenide glass layer (17); and applying a conditioning pulse to the memory element to bond regions of metal and glass within

said chalcogenide glass layer (page 1, paragraphs 3-5; page 2, paragraph 27), said bonded regions forming at least one conducting channel within said chalcogenide glass layer (page 1, paragraphs 3-5). Campbell discloses usage of germanium-selenide glass doped with silver for resistance variable material, the examiner takes the position that the step of forming a conducting channel or a dendrite within the resistance variable material under the influence of the applied voltage is inherently performed (page 1, paragraphs 3-5).

11. With respect to claim 62, Campbell discloses a method of forming a memory element as set forth in claim 61, wherein said resistance variable material layer is a chalcogenide glass layer (page 2, paragraph 25).

12. With respect to claim 63, Campbell discloses a method of forming a memory element as set forth in claim 62, wherein said chalcogenide glass layer has a stoichiometry of Ge_xSe_{100-x} (page 2, paragraph 26).

13. With respect to claim 96, Campbell discloses a method of forming a memory element as set forth in claim 89, further comprising forming a metal-containing layer (18) over said doped chalcogenide glass layer (17; page 2, paragraph 27).

14. With respect to claim 97, Campbell discloses a method of forming a memory element as set forth in claim 96, wherein said metal-containing layer comprises silver (page 2, paragraphs 27 and 29).

15. With respect to claim 98, Campbell discloses a method of forming a memory element as set forth in claim 97, wherein said metal-containing layer provides metal ions that move in and out of the conducting channel (page 1, paragraphs 3-6). Campbell discloses the germanium selenide glass receives silver ions through an adjacent silver selenide layer with applied voltage (page 1, paragraphs 3-6). The examiner takes the

position that it is inherent that when a positive write voltage is applied, the silver ions are driven into a conductive dendrite, and when a negative destructive read voltage is applied, the silver ions are driven out of the conductive dendrite (page 3, paragraphs 36 and 37).

16. With respect to claim 113, Campbell discloses a method of forming a memory element as set forth in claim 99, further comprising forming a second chalcogenide glass layer (fig. 2, item 117) over said at least one metal-containing layer (fig. 2, item 18).

17. With respect to claim 114, Campbell discloses a method of forming a memory element as set forth in claim 113, wherein said second chalcogenide glass layer is from about 100 Å to about 300 Å thick (pages 2 and 3, paragraph 32).

18. With respect to claim 115, Campbell discloses a method of forming a memory element as set forth in claim 114, further comprising forming a second metal-containing layer (fig. 2, item 118) over said second chalcogenide glass layer (fig. 2, item 117).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

19. Claims 64-72, 77-82, 84-88, 90-92, 100-106, 110-112, and 116-119 are rejected under 35 U.S.C. 103(a) as being unpatentable over Campbell.

20. With respect to claims 64 and 91, Campbell discloses a method of forming a memory element as set forth in claims 63 and 89, but Campbell does not disclose expressly wherein said doped chalcogenide glass layer has a stoichiometry from about $Ge_{18}Se_{82}$ to $Ge_{25}Se_{75}$. However, Campbell discloses the stoichiometry of the doped chalcogenide glass layer from about $Ge_{18}Se_{82}$ to $Ge_{43}Se_{57}$ (page 2, paragraphs 26-27). Since the claimed range and the part of Campbell's stoichiometry range are overlapping, the examiner takes the position that it is obvious that the claimed limitation is met.

21. With respect to claim 65, Campbell discloses a method of forming a memory element as set forth in claim 64, wherein said chalcogenide glass layer is doped with metal ions (page 2, paragraph 27).

22. With respect to claim 66, Campbell discloses a method of forming a memory element as set forth in claim 65, wherein said metal ions are silver ions (page 2, paragraph 27).

23. With respect to claim 67, Campbell discloses a method of forming a memory element as set forth in claim 66, wherein said doped chalcogenide glass layer is from about 150 Å to about 600 Å thick (page 2, paragraphs 26-27).

24. With respect to claim 68, Campbell discloses a method of forming a memory element as set forth in claim 67, wherein said doped chalcogenide glass layer has polarizable metal-chalcogen regions (page 2, paragraph 27). Campbell discloses usage of germanium-selenide glass doped with silver for resistance variable material, the examiner takes the position that the step of forming polarizable metal-chalcogen region, which is silver selenide region, and glass backbone region (page 2, paragraph 27) is inherently performed.

25. With respect to claims 69 and 90, Campbell discloses a method of forming a memory element as set forth in claims 68 and 89, wherein said polarizable metal-chalcogen regions are Ag_2Se regions within a germanium-selenide glass backbone (page 2, paragraph 27).

26. With respect to claim 70, Campbell discloses a method of forming a memory element as set forth in claim 69, but Campbell does not disclose expressly wherein said Ag_2Se regions become aligned upon application of said conditioning voltage to said memory element. Since Campbell teaches the silver doped germanium selenide glass layer that contains polarizable silver selenide regions and glass backbone regions (page 2, paragraph 27) forms a conductive dendrite by applying voltage (page 1, paragraphs 3-5), the examiner takes the position that the steps of becoming silver selenide regions aligned under the influence of the applied voltage is inherent due to the presence of an electric field caused by the applied voltage.

27. With respect to claim 71, Campbell discloses a method of forming a memory element as set forth in claim 70, but Campbell does not disclose expressly wherein said conditioning voltage is greater than subsequent write, read, and erase voltages. According to Campbell, a conductive dendrite or filament grows under influence of the applied voltage to extend between the electrodes, effectively interconnecting the two electrodes (page 1, paragraph 3). Subsequent write, read, and erase voltages need to be applied without shorting the memory element, and the conditioning voltage that allow a dendrite to connect two electrodes is the maximum voltage without shorting the memory element. So, the examiner takes the position that it is obvious that the amount of voltage required to grow a dendrite completely through the ion conductor and connect the electrodes is greater than subsequent write, read, and erase voltages.

28. With respect to claims 72 and 92, Campbell discloses a method of forming a memory element as set forth in claims 70 and 90, but Campbell does not disclose wherein the Ag_2Se regions form at least one conducting channel by becoming polarized and aligning within the doped chalcogenide glass layer. Since Campbell teaches the silver doped germanium selenide glass layer that contains polarizable silver selenide regions and glass backbone regions (page 2, paragraph 27) forms a conductive dendrite by applying voltage (page 1, paragraphs 3-5), the examiner takes the position that the steps of becoming polarized and aligning silver selenide regions under the influence of the applied voltage is inherent due to the presence of an electric field caused by the applied voltage.

29. With respect to claims 77 and 100, Campbell discloses a method of forming a memory element as set forth in claims 61 and 99, but Campbell does not disclose expressly wherein said chalcogenide glass layer has a stoichiometry from about $Ge_{20}Se_{80}$ to $Ge_{43}Se_{57}$. However, Campbell discloses the stoichiometry of the doped chalcogenide glass layer from about $Ge_{18}Se_{82}$ to $Ge_{43}Se_{57}$ (page 2, paragraphs 26). Since the claimed range and the part of Campbell's stoichiometry range are overlapping, the examiner takes the position that it is obvious that the claimed limitation is met.

30. With respect to claims 78 and 101, Campbell discloses a method of forming a memory element as set forth in claims 77 and 100, wherein said chalcogenide glass layer has a stoichiometry of $Ge_{40}Se_{60}$ (page 2, paragraph 26).

31. With respect to claims 79 and 102, Campbell discloses a method of forming a memory element as set forth in claims 77 and 100, wherein said chalcogenide glass layer is from about 150 Å to about 500 Å thick (page 2, paragraph 26).

32. With respect to claims 80 and 103, Campbell discloses a method of forming a memory element as set forth in claims 61 and 99, but Campbell does not disclose expressly wherein said at least one metal-containing layer is from about 300 Å to about 1200 Å thick. Campbell discloses the preferable ratio of silver-selenide layer thickness to first chalcogenide glass layer thickness is between about 2:1 and about 3.1:1 (page 2, paragraph 30). That means that the metal-containing layer thickness is between about 300 Å to about 465 Å, since the most preferable chalcogenide glass layer thickness is about 150 Å (page 2, paragraph 26). Since part of the claimed thickness range and the Campbell's metal-containing thickness range are overlapping, the examiner takes the position that it is obvious that the claimed limitation is met.

33. With respect to claims 81 and 104, Campbell discloses a method of forming a memory element as set forth in claims 80 and 103, wherein said at least one metal-containing layer is an Ag_2Se layer (page 2, paragraphs 20, 27 and 29).

34. With respect to claim 82, Campbell discloses a method of forming a memory element as set forth in claim 81, wherein the conditioning voltage is applied to the memory element driving Ag_2Se into the chalcogenide glass layer (page 1, paragraphs 3-5; page 2, paragraph 27).

35. With respect to claims 84 and 105, Campbell discloses a method of forming a memory element as set forth in claims 83 and 102, wherein the chalcogenide glass layer has a germanium-selenide glass backbone (page 2, paragraphs 26-27).

36. With respect to claims 85 and 106, Campbell discloses a method of forming a memory element as set forth in claims 84 and 105, wherein the Ag_2Se bonds to the germanium-selenide glass backbone (page 2, paragraphs 26-27) forming at least one conducting channel within said chalcogenide glass layer (page 1, paragraphs 3-5).

37. With respect to claims 86 and 110, Campbell discloses a method of forming a memory element as set forth in claims 80 and 99, further comprising forming a second metal-containing layer over the first metal-containing layer (page 3, paragraph 38).

38. With respect to claims 87 and 111, Campbell discloses a method of forming a memory element as set forth in claims 86 and 110, wherein said second metal-containing layer comprises silver ions (page 3, paragraph 38).

39. With respect to claims 88 and 112, Campbell discloses a method of forming a memory element as set forth in claims 87 and 111, wherein said silver ions are driven into and out of the at least one conducting channel (page 1, paragraphs 3-6) by applying a write, erase or read voltage (page 3, paragraphs 36-37). Campbell discloses the germanium selenide glass receives silver ions through an adjacent silver selenide layer with applied voltage. The examiner takes the position that it is inherent that when a positive write voltage is applied, the silver ions are driven into a conductive dendrite, and when a negative destructive read voltage is applied, the silver ions are driven out of the conductive dendrite.

40. With respect to claim 116, Campbell discloses a method of forming a memory element as set forth in claim 115, but Campbell does not disclose expressly wherein said second metal-containing layer is from 100 Å to about 500 Å thick. Campbell discloses the preferable total thickness of the combined metal-containing layers thickness is between about 2 to 3.3 times greater than the thickness of the first chalcogenide glass layer and the second chalcogenide glass layer (page 3, paragraph 39). That means that the total thickness of the combined metal-containing layers is between about 600 Å to about 990 Å, since the most preferable thickness for first and second chalcogenide glass layers is about 150 Å (page 2, paragraphs 26 and 32). So,

second metal-containing layer thickness is between about 300 Å to 525 Å because the thickness of first metal-containing layer is between about 300 Å to 465 Å. Since part of the claimed thickness range and the Campbell's second metal-containing thickness range are overlapping, the examiner takes the position that it is obvious that the claimed limitation is met.

41. With respect to claim 117, Campbell discloses a method of forming a memory element as set forth in claim 116, further comprising forming a third metal-containing layer over said second metal-containing layer. According Campbell, any number of silver-selenide layers may be used. Thus, an optional second silver-selenide layer may be deposited on the first silver-selenide layer (page 3, paragraphs 38). The examiner takes the position that it is obvious that forming a third metal-containing layer over second metal-containing layer since the second metal-containing layer may be formed on the first metal-containing layer.

42. With respect to claim 118, Campbell discloses a method of forming a memory element as set forth in claim 117, wherein said third metal-containing layer comprises silver ions (page 3, paragraphs 38).

43. With respect to claim 119, Campbell discloses a method of forming a memory element as set forth in claim 118, wherein said silver ions are driven into and out of at least one conducting channel (page 1, paragraphs 3-6) by applying a write, erase, or read voltage (page 3, paragraphs 36-37). Campbell discloses the germanium selenide glass receives silver ions through an adjacent silver selenide layer with applied voltage. The examiner takes the position that it is obvious that when a positive write voltage is applied, the silver ions are driven into a conductive dendrite, and when a negative

destructive read voltage is applied, the silver ions are driven out of the conductive dendrite.

44. Claims 74-76, 94, 95, and 108-109 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kozicki.

45. With respect to claim 74, Kozicki discloses a method of forming a memory element as set forth in claim 73, but Kozicki does not disclose expressly wherein subsequent write, read, and erase voltages have an absolute magnitude lower than that of said conditioning voltage. According to Kozicki, a dendrite grows when a voltage is applied and it may be allowed to grow until it connects two electrodes (col. 5, lines 51-67). Subsequent write, read, and erase voltages need to be applied without shorting the memory element, and the conditioning voltage that allow a dendrite to connect two electrodes is the maximum voltage without shorting the memory element. So, the examiner takes the position that it is obvious that the absolute magnitude of subsequent write, read, and erase voltages is lower than the conditioning voltage required to grow a dendrite completely through the ion conductor and connect the electrodes.

46. With respect to claims 75, 76, 94, 95, 108, and 109, Kozicki discloses a method of forming a memory element as set forth in claims 74, 93, and 107, but Kozicki does not disclose expressly wherein applying a write voltage produces a third resistance state lower than the second resistance state; and applying a second write voltage produces a fourth resistance state lower than said third resistance state. According Fig. 2, Kozicki discloses greater changes in the resistance value are achieved when larger voltages are used (col. 6, lines 55-67). After achieving second resistant state, which is lower than the resistant state before any voltage is applied (as shown in Fig. 2), if a

write voltage is applied then the resistant value will decrease more achieving third low resistant state lower than the second resistant state. After third resistant state, if another write voltage is applied, again the resistant value will decrease achieving fourth low resistant state lower than third resistant state. Adding up all the voltages applied in a memory element results a big change of resistant value from the first high resistant state.

47. Claim 83 is rejected under 35 U.S.C. 103(a) as being unpatentable over Campbell in view of Kozicki.

With respect to claim 83, Campbell discloses a method of forming a memory element as set forth in claim 82, but Campbell does not disclose expressly wherein said conditioning voltage has a pulse duration of from about 10 to about 500 ns and greater than about 700 mV. However, any variation in conditioning voltage in the present claim is obvious in light of the cited art, because the changes in conditioning voltage produce no unexpected function. The conditioning voltage parameter depends on the thickness of the memory element. The larger width of memory element requires higher conditioning voltage and longer time. Also, according to Kozicki, the growth rate of a conductive channel or a dendrite is a function of the conditioning voltage and time (col. 6, lines 32-42). Low voltages result in relatively slow growth whereas higher voltages produce rapid growth. The examiner takes the position that it is obvious that the conditioning voltage parameters are not fixed values.

Response to Arguments

In view of applicant's arguments the restriction requirement has been withdrawn.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cheung Lee whose telephone number is 571-272-5977. The examiner can normally be reached on Monday through Friday from 8:30AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Cheung Lee

August 4, 2005

HA NGUYEN
PRIMARY EXAMINER